Improved Subthreshold Swing and Gate-Bias Stressing Stability of p-Type Cu_2O Thin-Film Transistors Using a HfO_2 High-k Gate Dielectric Grown on a SiO_2/Si Substrate by Pulsed Laser Ablation

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***Abstract*—p-Type Cu_2O thin films and HfO_2 high-k gate dielectrics are deposited by pulsed laser ablation. p-Type Cu_2O metal–oxide–semiconductor capacitors and thin-film transistors (TFTs) are then fabricated and investigated. Experimental results show that a HfO_2/SiO_2-stacked gate dielectric can effectively improve interface properties and decrease gate-leakage current when compared with a SiO_2 gate dielectric. Thus, increased mobility, a decreased subthreshold swing, and enhanced gate-bias-voltage stressing stability have been achieved for the relevant Cu_2O TFTs. Bottom-gate and top-source/drain-contact p-channel Cu_2O TFTs ($W/L = 500/20\ \mu m$) with the HfO_2/SiO_2-stacked gate dielectric exhibit superior performance with a saturation-carrier-mobility value of 2.7 $cm^2/V \cdot s$, an ON–OFF current ratio of 1.5×10^6, a subthreshold swing of 137 mV/dec, and a threshold-voltage shift of 1.4 V after gate-bias stress at 10 V for 3600 s.**

***Index Terms*—Cu_2O, HfO_2, stressing stability, subthreshold swing, thin-film transistors (TFTs).**

I. Introduction

TRANSPARENT conducting oxides (TCOs) have attracted wide interest in electronic and optoelectronic devices. Most of the TCOs are n-type semiconductors such as ZnO, In_2O_3, and InGaZnO. It has been proven to be very difficult to develop reproducible methods for the p-type doping of these materials. However, p-type TCO materials are also required because the fabrication of complementary metal–oxide–semiconductor (MOS) integrated circuits needs both n-type and p-type transistors [1]. Copper oxides including cuprous oxide (Cu_2O) and cupric oxide (CuO) have a native p-type property owing to the presence of Cu vacancies, which introduce an acceptor level [2]. In particular, Cu_2O has the potential as a channel material for high-speed and low-power thin-film transistors (TFTs) because of its high carrier mobility for large drive current and its appropriate bandgap (i.e., 2.0–2.6 eV) for supply-voltage scaling [3], [4]. However, Cu_2O-based transistors have been reported with unsatisfactory performance up to now. Matsuzaki *et al.* [5] investigated a Cu_2O TFT with 150-nm Al_2O_x gate dielectric, but its field-effect mobility and its ON–OFF current ratio were $\sim$0.26 $cm^2/V \cdot s$ and $\sim$6, respectively. Fortunato *et al.* [1] reported p-type Cu_2O TFTs fabricated at room temperature, using 220-nm ATO (i.e., the superlattice of Al_2O_3 and TiO_2) as a gate dielectric; a field-effect mobility value of 1.2×10^{-3} $cm^2/V \cdot s$ and an ON–OFF current ratio of 2×10^2 were achieved. The device performance of the TFTs aforementioned was limited probably due to their gate dielectric, which provided insufficient gate-capacitance density and an imperfect channel/gate-dielectric interface. We fabricated a polycrystalline-Cu_xO (including Cu_2O and CuO) MOS capacitor with a 12-nm HfO_2/SiO_2-stacked gate dielectric [6] and obtained a slightly high interface-state density of $\sim 10^{12}$ cm^{-2} eV^{-1}, which resulted from the scatterings of both the ionized defect and the grain boundary. We also obtained a saturation mobility value of 4.3 $cm^2/V \cdot s$ and an ON–OFF current ratio of 3×10^6 for pure polycrystalline-Cu_2O TFTs with a thin HfON high-k gate dielectric [7]. Nevertheless, a lack of saturation of the I–V characteristics attributed to large gate leakage is a main obstacle to the practical use of such a device. This paper reports the fabrication and the characterization of MOS capacitors and TFTs based on p-type Cu_2O thin films deposited by pulsed laser ablation. The HfO_2/SiO_2 stack is used as a gate dielectric to reduce the gate-leakage current [8], [9]. The Cu_2O MOS capacitor with the HfO_2/SiO_2-stacked dielectric

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shows a high gate-capacitance density of ∼140 pF/cm^2 and a low interface-state density of 6.7×10^{11} eV^{-1}cm^{-2}. The bottom-gate $Cu_2O/HfO_2/SiO_2$ TFT exhibits a high saturation mobility value of 2.7 cm^2/V · s and a small subthreshold swing of 137 mV/dec due to its improved interface properties and its reduced gate-leakage current. The gate-bias-voltage stressing is also performed to inspect the stability of Cu_2O TFTs. The threshold-voltage shift after stressing the $Cu_2O/HfO_2/SiO_2$ TFT is lower than that of the Cu_2O/SiO_2 TFT after stress, indicating that the trap states located at the channel/gate-dielectric interface are effectively suppressed by the application of HfO_2 dielectric film.

II. Experimental Details

SiO_2 was first thermally grown on p$^+$-silicon wafers followed by a standard RCA cleaning process. To investigate the properties of the gate-dielectric/channel interface, Cu_2O MOS capacitors with a HfO_2/SiO_2-stacked gate dielectric were fabricated. HfO_2 with a nominal thickness of 100 nm was deposited on a SiO_2 (10 nm)/Si substrate in pure O_2 by sputtering a HfO_2 target (4N) in a pulsed-laser-deposition (PLD) system at room temperature. PLD is widely used to prepare high-quality metal–oxide thin films because the films deposited usually have homogeneous stoichiometry and a smooth surface. Prior to deposition, the chamber was pumped down to a base pressure below 1×10^{-4} Pa. A KrF excimer laser was used as the laser source with the following parameters: a wavelength of 248 nm, a pulse duration of 20 ns, a pulse frequency of 7 Hz, a laser power density of 2 mJ · cm^{-2} at the target surface, and a beam incident angle of 45°. Subsequently, a Cu_2O film with a nominal thickness of 300 nm was *in situ* deposited on HfO_2 at a substrate temperature of 500 °C [7] with a Cu metal target (4N) and an oxygen partial pressure of 0.6 Pa. Then, Pt was deposited on Cu_2O to ensure the ohmic contact for the electrical-characteristic measurement. Finally, Al was thermally evaporated and patterned as a gate-contact electrode on the back of p$^+$ Si, followed by forming-gas annealing at 300 °C for 20 min. The Cu_2O MOS capacitors with a HfO_2/SiO_2-stacked dielectric were prepared to measure the capacitance–voltage (C–V) characteristics and gate-leakage current, where the gate-bias voltage was applied to the Al-contact electrode, and the Pt electrode was grounded. For the preparation of TFTs, 100-nm HfO_2 was deposited on the SiO_2 (10 nm)/Si substrate, and the channel film of 40-nm Cu_2O was grown on HfO_2. Then, 100-nm Pt source/drain (S/D) electrodes were deposited on the Cu_2O film by conventional photolithography and by a liftoff process to achieve a channel width/length of 500/20 μm. As a result, bottom-gate top-contact Cu_2O TFTs were achieved. The Cu_2O MOS capacitors and TFTs with a 110-nm SiO_2 gate dielectric were also fabricated to compare their performance with those having a HfO_2/SiO_2-stacked gate dielectric.

The deposition rate as well as the typical film thickness was monitored by a quartz-crystal thickness monitor (TM-400, Maxtek, U.S.), whereas the gate-dielectric film thickness was checked by a VASE series multiwavelength ellipsometer. The surface morphology of the gate-dielectric film was observed by an atomic force microscope (AFM) (SPM-9500J3, Shimadzu, Japan). High-frequency (HF, 1-MHz) C–V characteristics were measured at room temperature using an HP4294A precision inductance–capacitance–resistance meter. Gate-leakage current for MOS capacitors and electrical properties for TFTs were measured by a Keithley 4200 precision semiconductor parameter analyzer. The average values of electrical parameters were calculated from the measured values of 16 devices, with four devices per wafer. All the electrical measurements were carried out under a light-tight and electrically shielded condition.

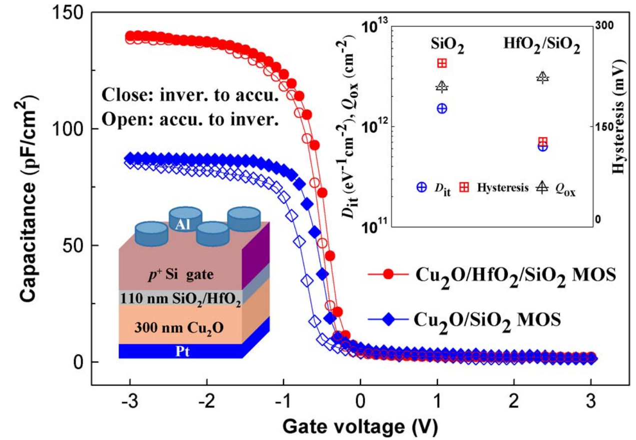

Fig. 1. Typical HF C–V curves for Cu_2O MOS capacitors swept in both directions at a frequency of 1 MHz. The inset (left) is the schematic diagram of the MOS capacitor. The inset (right) is the hysteresis, the interface-state density, and the equivalent oxide charge density extracted from the HF C–V curve.

III. Results and Discussion

Fig. 1 depicts the typical HF C–V curves for the MOS capacitors. The schematic diagram of the MOS capacitor is shown in the inset (left) in Fig. 1. The accumulation capacitance (i.e., the gate-dielectric capacitance density C_{ox}) of the SiO_2 gate-dielectric capacitor is lower than that of the HfO_2/SiO_2-stacked gate-dielectric capacitor, which is attributed to the high permittivity of the HfO_2/SiO_2 dual-layer dielectric film. The electrical parameters of the MOS capacitor, such as hysteresis voltage, the equivalent oxide charge density Q_{ox} calculated by $-C_{\mathrm{ox}} \times (V_{\mathrm{fb}} - \varphi_{\mathrm{ms}})/q$ [10], and the interface-state density D_{it} near the midgap estimated from the HF C–V curve by the Terman method [11] for comparison purposes are all shown in the inset (right) in Fig. 1. The hysteresis voltage of the MOS capacitor with the SiO_2 gate dielectric is 240 mV, which is larger than that of the capacitor with the HfO_2/SiO_2-stacked gate dielectric (110 mV), indicating more charge trapping at the Cu_2O/SiO_2 interface. The D_{it} of the Cu_2O MOS capacitor with the HfO_2/SiO_2-stacked dielectric is about 6.7×10^{11} eV^{-1}cm^{-2} and is lower than that of the MOS capacitor with the SiO_2 gate dielectric. Furthermore, the D_{it} of the $Cu_2O/HfO_2/SiO_2$ MOS capacitor is also lower than that of the mixed Cu_xO (Cu_2O plus CuO)/HfO_2/SiO_2 capacitor (∼10^{12} eV^{-1} cm^{-2}) reported in [6], indicating that the stoichiometry of the channel film has significant effects on the interface properties.

The transfer characteristics (I_{DS} versus V_{GS} at $V_{DS} =$ 4 V) and the gate-leakage current of the Cu_2O TFTs with

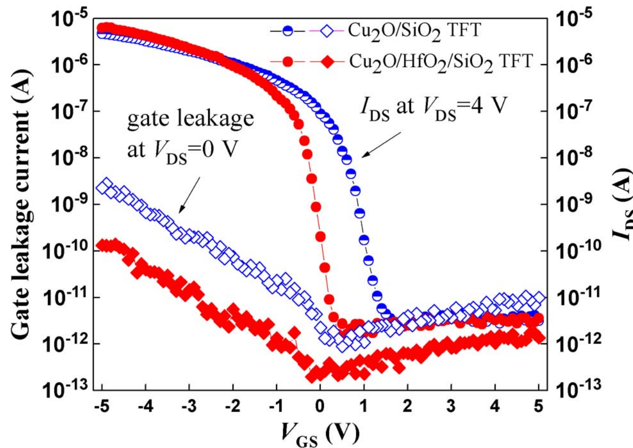

Fig. 2. Transfer characteristics of Cu_2O TFTs ($W/L = 500\ \mu m/20\ \mu m$) with the HfO_2/SiO_2-stacked gate dielectric and the SiO_2 gate dielectric, respectively. V_{GS} was swept from 5 to -5 V, at $V_{DS} = 4$ V and a gate-leakage current of Cu_2O TFTs. V_{GS} was swept from 5 to -5 V, at $V_{DS} = 0$ V.

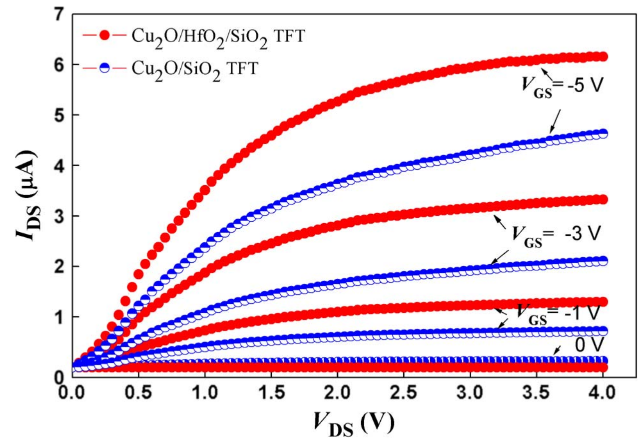

Fig. 3. Output characteristics of Cu_2O TFTs ($W/L = 500\ \mu m/20\ \mu m$) with the HfO_2/SiO_2-stacked gate dielectric and the SiO_2 gate dielectric, respectively. V_{DS} was swept from 0 to 4 V at $V_{GS} = -5, -3, -1$, and 0 V.

$W/L = 500\ \mu m/20\ \mu m$ are shown in Fig. 2. All TFTs show a p-channel transistor behavior. The $Cu_2O/HfO_2/SiO_2$ TFT exhibits enhancement-mode characteristics with completely turned-off current at $V_{GS} = 0$ V. The Cu_2O/SiO_2 TFT operates in depletion mode due to a high drain/source current of 140 nA at $V_{GS} = 0$ V, which is unfavorable for low-power circuits. For the Cu_2O TFT with a HfO_2/SiO_2-stacked dielectric, the drain current is about 6×10^{-6} A at a gate voltage of -5 V and a drain voltage of $+4$ V in the ON state, whereas it is $\sim 4 \times 10^{-12}$ A in the OFF state, corresponding to an ON–OFF current ratio of 1.5×10^6. The saturation mobility μ_{sat} is extracted from a linear fitting to the $(I_{DS})^{1/2}$–V_{GS} curve, which is based on the following:

$$I_{DS} = (\mu_{sat} C_{ox} W/2L)(V_{GS} - V_{TH})^2$$

where V_{TH} is the threshold voltage estimated by the intercept of the extrapolated curve with the voltage axis. The $Cu_2O/HfO_2/SiO_2$ TFT exhibits a peak mobility value of $2.7\ cm^2/V \cdot s$, whereas the Cu_2O/SiO_2 TFT has a μ_{sat} value of $0.43\ cm^2/V \cdot s$. This should be mainly attributed to an enhanced hole scattering arising from more interface states and larger oxide leakage and from the small gate capacitance of the SiO_2 gate dielectric. The subthreshold slope S is estimated by the $[\partial(\log I_{DS})-\partial V_{GS}]^{-1}$ curve. The $Cu_2O/HfO_2/SiO_2$ TFT shows an S value of 137 mV/dec, whereas the S value of Cu_2O/SiO_2 TFT degrades to 315 mV/dec, owing to a high trap-state density at the Cu_2O/SiO_2 interface, which is in agreement with the results of the MOS capacitors aforementioned. The S value of the $Cu_2O/HfO_2/SiO_2$ TFT is smaller than that of the Cu_2O TFT with the HfON gate dielectric (0.18 V/dec) reported in [7], but it does not demonstrate that the Cu_2O/HfO_2 interface is superior to the Cu_2O/HfON interface. Gate leakage should be a potential origin for the deteriorated subthreshold swing of the Cu_2O TFT with the HfON gate dielectric, and the underlying mechanisms need to be further explored. The gate-leakage property as a function of V_{GS} is measured at $V_{DS} = 0$ V and is shown in Fig. 2. For the TFT with the SiO_2 gate dielectric, the maximum OFF-state current is less than 8×10^{-12} A, and it mainly comes from the gate-leakage current. In the ON state, the gate-leakage current contributes less than 0.1% of the drain current at the same gate-bias voltage. However, for the TFT with the HfO_2/SiO_2-stacked dielectric, the gate leakage is less than the OFF-state current (about one order of magnitude). The gate-leakage current in the ON state is lower by four orders of magnitude than the drain current, which indicates that the impact of gate leakage on the electrical characteristics of the TFT with the HfO_2/SiO_2-stacked dielectric can be ignored. The gate leakage is slightly high for the TFTs due to the application of a common gate. If the gate electrode is patterned as a small area, then the gate leakage should be drastically reduced. We have measured the surface roughness of SiO_2 and HfO_2 grown on the Si substrate by AFM as 1.54 and 3.37 nm, respectively, but the SiO_2 sample has a higher gate leakage. Therefore, the low gate-leakage current is not dominantly determined by the small surface roughness of the gate dielectric. The reduced gate-leakage current of the HfO_2/SiO_2-stacked dielectric should be ascribed to the improved interface quality (low interface-state density and/or trap density) and superior bulk insulating property of the HfO_2 thin film.

The output characteristics (i.e., the drain current I_{DS} versus the D/S voltage V_{DS} at the constant gate/source voltage V_{GS}) of the Cu_2O TFTs are shown in Fig. 3. The $Cu_2O/HfO_2/SiO_2$ TFT shows larger I_{DS} than the Cu_2O/SiO_2 TFT, which should be attributed to the larger gate-dielectric capacitance and higher saturation mobility. Drain-current saturation can be observed at high D/S voltage for the $Cu_2O/HfO_2/SiO_2$ TFT, indicating that the gate bias and the D/S voltage have a particular control capability for the Fermi level in the channel. However, the pinning of the Fermi level at the Cu_2O/HfO_2 interface is not effectively suppressed, which can be presumed from the relatively low saturation mobility, compared with the Hall mobility $\sim 100\ cm^2/V \cdot s$ of the Cu_2O film [7]. An inadequate saturation behavior is obviously found for the Cu_2O/SiO_2 TFT at $V_{GS} = -5$ V, indicating an incomplete pinchoff of the channel layer, which should be ascribed to the high gate-leakage current. Moreover, the TFTs show current crowding in the low V_{GS} region, which implies high resistivity of the S/D contact [12]. The width-normalized R_{SD} is roughly estimated to be

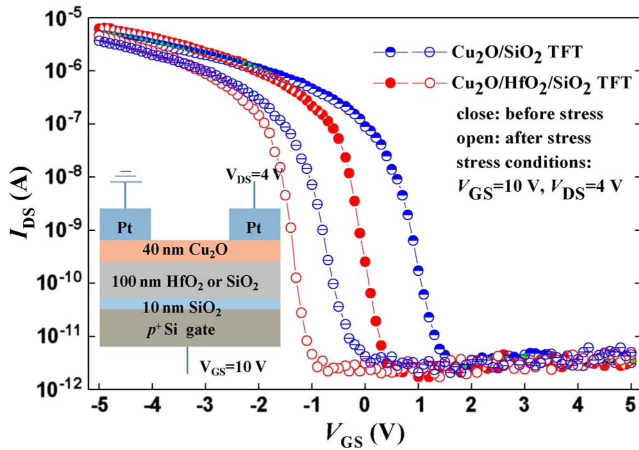

Fig. 4. Evolution of the transfer-characteristic curves after gate-bias-voltage stressing for Cu_2O TFTs with the HfO_2/SiO_2-stacked gate dielectric and the SiO_2 gate dielectric, respectively. Stressing conditions: $V_{GS} = 10$ V, $V_{DS} = 4$ V, and stressing duration = 3600 s. The inset is the schematic diagram for the stressing test.

1100–1300 Ωcm, which is too high to avoid the kink current in the low-gate-voltage region. Relevant studies on reducing the contact resistance by inserting a high conductive interlayer between the S/D metal electrode and the Cu_2O channel are underway.

Fig. 4 shows the gate-bias stressing stability of the Cu_2O TFTs. The measurement is performed at room temperature in air, with $V_{DS} = 4$ V, and stressing duration = 3600 s. The gate-bias stressing condition is V_{GS} at 10 V, and a positive gate bias is applied to set the TFT in the OFF state [13]. 10 V is selected to ensure that the HfO_2 and SiO_2 layers are all under the breakdown field [14]. The inset in Fig. 4 is the schematic diagram for the stressing stability test of the Cu_2O TFTs. After stress, the transfer characteristics of the transistors are recorded at a D/S voltage of 4 V by sweeping the gate bias from −5 to 5 V, whereas the source electrode is grounded. For all TFTs, the transfer curve shifts in the negative direction after stressing, but the slope of the transfer curve does not show a large difference indicating that the shift after stress can be mainly ascribed to the change in the threshold voltage $\Delta V_{\rm TH}$, whereas the creation of electron trapping states at the channel/gate-dielectric interface after the gate-bias stressing can be neglected. The Cu_2O TFTs with a HfO_2/SiO_2 gate stack and with only SiO_2 show an initial $V_{\rm TH}$ value of 0.3 and 1.2 V, respectively. The value of $\Delta V_{\rm TH}$ for the $Cu_2O/HfO_2/SiO_2$ and Cu_2O/SiO_2 TFTs is about 1.4 and 2.2 V, respectively, indicating that the trap states density located at the Cu_2O/SiO_2 interface or in the SiO_2 layer is higher than at the Cu_2O/HfO_2 interface or in the HfO_2 layer.

Thus, it can be suggested that the Cu_2O TFT with the HfO_2/SiO_2-stacked dielectric has significantly improved interface properties and thus effectively enhanced saturation mobility. The $Cu_2O/HfO_2/SiO_2$ TFT shows higher saturation mobility and a larger ON–OFF current ratio than those reported in [1] and [4]. The mobility and the ON–OFF current ratio of the present TFT are slightly lower than our previous results [7]. However, the $Cu_2O/HfO_2/SiO_2$ TFT demonstrates distinct improvements in output characteristics, subthreshold swings, and gate-bias stressing stability.

IV. Conclusion

In summary, Cu_2O and HfO_2 high-k gate-dielectric films are grown by PLD and then used to fabricate Cu_2O MOS capacitors and TFTs. The MOS capacitors with a HfO_2/SiO_2-stacked gate dielectric show superior electrical properties, such as low interface-state density and small gate-leakage current. Bottom-gate Cu_2O TFTs with a HfO_2/SiO_2-stacked gate dielectric exhibit good output and transfer characteristics, yielding sixfold hole mobility enhancement when compared with that of the SiO_2 gate dielectric. Nevertheless, Fermi-level pinning at the interface and drain-current crowding in the low-voltage region are not effectively suppressed in this paper. It is expected that the optimum conditions for the fabrication of Cu_2O TFTs can be obtained by reducing the S/D contact resistance (by inserting a highly conductive interlayer between the metal electrode and the active channel) and improving the quality of the Cu_2O film and the channel/gate-dielectric interface. As a result, the performance of the Cu_2O TFTs can be probably enhanced to a commercially usable level.

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