High-Performance Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors With $HfO_xN_y/HfO_2/HfO_xN_y$ Tristack Gate Dielectrics

Longyan Yuan, Xiao Zou, Guojia Fang, Jiawei Wan, Hai Zhou, and Xingzhong Zhao

***Abstract*—We have fabricated and investigated amorphous indium gallium zinc oxide (α-IGZO) thin-film transistors (TFTs) by using $HfO_xN_y/HfO_2/HfO_xN_y$ (NON) as the gate dielectric. The NON tristack dielectric structure can increase the gate capacitance density, effectively improve interface properties of both the gate/dielectric and dielectric/active channels, suppress the charge trap density, and reduce the gate leakage. The α-IGZO TFT ($W/L = 200/10\ \mu m$) with NON shows superior performance such as a saturation current of 0.33 mA, an ON/OFF-current ratio of 2.2×10^6, a saturation mobility of 10.2 $cm^2/V \cdot s$, a source/contact resistivity of 83 $\Omega \cdot cm$, a subthreshold swing of 0.13 V/dec, and enhanced stressing reliability.**

***Index Terms*—Amorphous, HfO_2, HfO_xN_y, high permittivity, indium gallium zinc oxide (IGZO), thin-film transistors (TFTs).**

I. Introduction

TRANSPARENT amorphous oxide semiconductors have attracted much attention as promising channel materials for low-temperature thin-film transistors (TFTs) because of their high field effect mobility of $\sim$10 $cm^2/V \cdot s$ even when fabricated at room temperature [1]. Amorphous indium gallium zinc oxide (α-IGZO) now has been considered as the most likely candidate for practical applications, such as flat-panel display and light-emitting diodes. Recently, much effort has been focused on low-power-consumption oxide-based TFTs with high-κ gate insulators [2]–[4]. HfO_2 is one of the most promising dielectric materials due to its high permittivity ($\kappa \sim 17$) and wide band gap (5.7 eV), and it can be fabricated at room temperature. However, HfO_2 tends to react with the substrate, forming a low-κ interface layer between HfO_2 and the substrate [5]. Furthermore, HfO_2 deteriorates the interface quality between HfO_2 and the channel layer in TFTs [6]. We had reported that the nitrogen incorporation into HfO_2 can improve interface properties and increase the gate capacitance density [7]. However, thermal-grown SiO_2 between the Si gate and dielectric leads to reduced equivalent κ value of stack gate dielectrics and increased gate leakage, so the interface between the active channel and gate should be further optimized.

In this letter, a novel $HfO_xN_y/HfO_2/HfO_xN_y$ (NON) tristack dielectric structure was applied to improve interface properties of both the gate/dielectric and the α-IGZO channel/dielectric. The NON α-IGZO TFT exhibited superior performance compared to the TFT using HfO_2 as the gate dielectric, such as high saturation mobility, small subthreshold swing, large ON/OFF-current ratio, and enhanced stressing reliability. Moreover, the drain saturation, subthreshold swing, and charge trap density of the TFT with NON were also improved compared to the TFT with the HfO_xN_y gate dielectric [7].

II. Experimental Details

A p-type (100) silicon ($0.1-0.5\ \Omega \cdot cm$) was used as the substrate, followed by a standard RCA cleaning process. A HfO_xN_y film with a nominal thickness of 10 nm was prepared by a radio frequency reactive magnetron sputtering system using an HfO_2 (99.9% pure) target at room temperature. The chamber was pumped down to $< 3 \times 10^{-4}$ Pa and backfilled with the sputtering gas to a pressure of 0.5 Pa. Mixtures of high-purity Ar (5 N) and N_2 (5 N) with a nitrogen flow ratio of 7% were introduced into the chamber by mass-flow controllers during the deposition. The sputtering power was kept at 100 W. HfO_xN_y films were deposited before and after the growth of HfO_2 to form a sandwichlike dielectric structure [8]. The nitrogen atomic concentration of the HfO_xN_y film was measured as 4.6% by XPS measurement. Here, the HfO_2 film with a nominal thickness of 130 nm was deposited at room temperature with Ar : O_2 = 3: 1. Thus, we prepared 10-nm HfO_xN_y/130-nm HfO_2/10-nm HfO_xN_y tristack dielectrics on the Si substrate. The α-IGZO channel material was deposited

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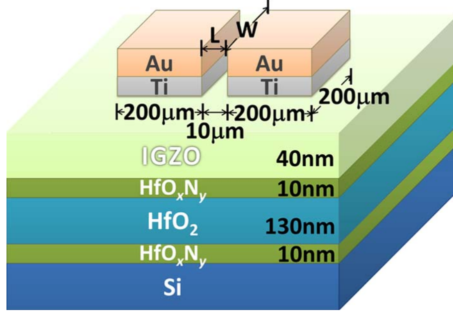

Fig. 1. Schematic diagram of an α-IGZO TFT with $HfO_xN_y/HfO_2/HfO_xN_y$ tristack dielectrics.

at room temperature by pulsed laser deposition with a KrF (248 nm) laser. The repetition rate of the laser with a pulse duration of 20 ns was 5 Hz, and the energy density was about 1.5 J/cm^2. Top-contact Ti/Au (40 nm/160 nm) source/drain (S/D) electrodes were formed by patterning and sputtering. The α-IGZO TFTs with 150-nm HfO_2 were also fabricated for comparison.

The surface chemical bonding states of the films were measured by X-ray photoelectron spectroscopy (XPS, VG Multilab 2000), which was performed with all peaks referenced to C 1s at 284.6 eV. The surface morphology of the film was observed by AFM (SPM-9500J3, Shimadzu, Japan). The electrical characterization of the TFTs was measured by Keithley 4200 SCS and Agilent 4294A.

III. Results and Discussion

Fig. 1 illustrates an α-IGZO TFT with a NON gate insulator. The TFT is the bottom gate with top-contact S/D electrodes. The α-IGZO active layer is about 40 nm, and the width-to-length ratio is 20 $(W/L = 200/10\ \mu\text{m})$.

Fig. 2(a) and (b) shows the typical output and transfer characteristics of α-IGZO TFTs with HfO_2 only and NON gate insulators. Some results derived from Fig. 2 are listed in Table I. The saturation current for the TFT with the NON dielectric is 0.33 mA at a bias of $V_{\text{DS}} = V_{\text{GS}} = 6$ V, which is obviously higher than that of the TFT with the HfO_2 dielectric due to its improved interface properties and increased gate capacitance density. The gate capacitance densities of the two dielectrics are 67.5 and 76 nF/cm^2 for HfO_2 and NON, respectively.

The transfer characteristic curves at $V_{\text{DS}} = 6$ V are shown in Fig. 2(b). The forward/backward hystereses in the transfer curves are about 2.9 and 0.9 V for the TFTs with HfO_2 and NON dielectrics, respectively. The small hysteresis voltage of the α-IGZO TFT with the NON dielectric indicates that the HfO_xN_y interlayer effectively suppresses the charge trap at the interfaces. The gate leakage current was measured at $V_{\text{DS}} =$ 0 V by patterning the Al contact electrode on the backside of the Si substrate with an area of 8×10^{-5} cm^2. As shown in Fig. 2(b), the HfO_2 TFT exhibits a magnitude of 8% higher leakage current than that of the NON TFT, which indicates superior interfacial and insulating properties of the NON tristack dielectric.

The saturation mobility (μ_{sat}) and threshold voltage (V_{th}) were derived from the liner fitting to the $I_{\text{DS}}^{1/2}$-versus-V_{GS} plot

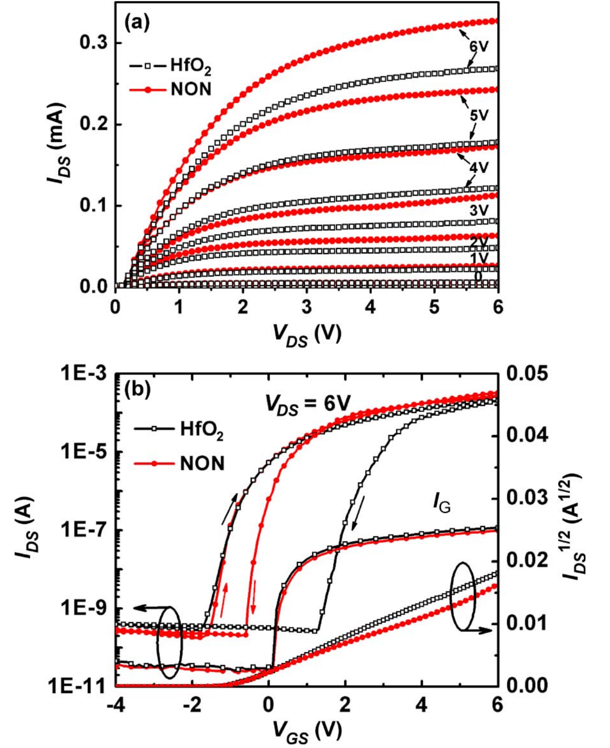

Fig. 2. Operation characteristics of α-IGZO TFTs with HfO_2 only and $HfO_xN_y/HfO_2/HfO_xN_y$ gate dielectrics, with $W/L = 200/10\ \mu$m. (a) Output characteristics. V_{DS} was swept from 0 to + 6 V at each V_{GS} varing from 0 to +6 V at 1 V step. (b) Transfer characteristics (@$V_{\text{DS}} = +6$ V) and gate leakage current (@$V_{\text{DS}} = 0$ V), V_{GS} was swept from −4 to +6 V.

TABLE I
EXTRACTED ELECTRICAL PARAMETERS OF α-IGZO TFTs WITH HfO_2 AND NON GATE DIELECTRICS

	V_{th} (V)	On/off ratio	SS (V/decade)	μ_{sat} (cm^2/V·s)
HfO_2	-1.0	1.2×10^6	0.24	8.4
NON	-0.92	2.2×10^6	0.13	10.2
SiO_2[10]	0.2	1.0×10^7	0.2	5
SiN_x[11]	2	5×10^7	0.5	5

using [9]

$$I_{\text{DS}} = \frac{\mu_{\text{sat}} C_i W}{2L} (V_{\text{GS}} - V_{\text{th}})^2 \tag{1}$$

where C_i is the gate dielectric capacitance density. The saturation mobility (μ_{sat}) and threshold voltage (V_{th}) are 8.4 cm^2/V · s and −1.0 V for the HfO_2 TFT and 10.2 cm^2/V · s and −0.92 V for the NON TFT, respectively. The absolute value of threshold for the NON TFT is slightly smaller than that of the HfO_2 TFT (−0.92 V), which means the reduced power consumption for the NON TFT is operating in the exhaustion model.

The subthreshold swing (SS) was estimated as 0.24 and 0.13 V/dec for the HfO_2 and NON TFTs, respectively. These results are relatively better than those of the α-IGZO TFTs with SiO_2 [10] and SiN_x [11] dielectrics. The trap charge density (N_{trap}) for TFTs can be determined as follows:

$$N_{\text{trap}} = \left(\frac{q \times SS}{k_B T \ln 10} - 1\right) \frac{C_i}{q} \tag{2}$$

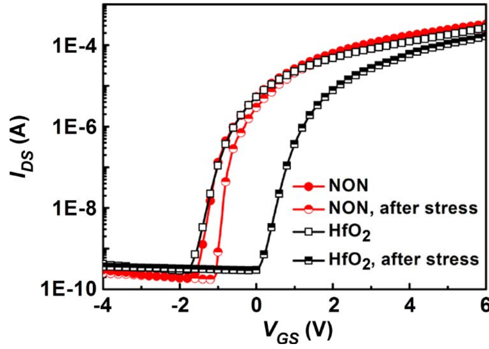

Fig. 3. Transfer curves before and after stress of 5 min for TFTs with NON and HfO_2 dielectrics. The gate bias voltage of 5 V was applied, and the S/D electrodes were grounded.

where q is the electronic charge, k_B is Boltzmann's constant, and T is the temperature. The $N_{\rm trap}$ values are approximately 5.6×10^{11} cm^{-2} and 1.3×10^{12} cm^{-2} for TFTs with NON and HfO_2 gate dielectrics, respectively. Small $N_{\rm trap}$ indicates that the trap charge is suppressed by the HfO_xN_y bi-interlayer, which further demonstrated the small hysteresis voltage of TFTs with NON tristack dielectrics previously mentioned.

Fig. 3 illustrates the transfer curves before and after a stress of 5 min for TFTs with NON and HfO_2 dielectrics. The gate bias voltage of 5 V was applied while the S/D electrodes were grounded. Positive $V_{\rm th}$ shifts after stressing can be observed with the unchanged subthreshold slope and saturation drain current. The large $V_{\rm th}$ shift (1.8 V) of the HfO_2 TFT shows more electrons trapping near/at the interface of the gate dielectric and active channel, while the $V_{\rm th}$ shift of 0.7 V indicates suppressed trap charge by using the NON tristack structure and reveals that the presence of the HfO_xN_y bi-interfacial layer could enhance the stressing reliability.

The saturation drain current strongly depends on the S/D contact resistivity between the channel and S/D metal electrodes for bottom-gate and top-contact TFTs [12]. The contact resistance $R_{\rm SD}$ can be evaluated by using the gated transmission line method in the liner region

$$R_{\rm TOT} = \frac{V_{\rm DS}}{I_{\rm DS}} = \frac{L}{\mu_{\rm sat} W C_i (V_{\rm GS} - V_{\rm th})} + R_{\rm SD}. \quad (3)$$

The width-normalized source–drain resistivity $(R_{\rm SD}W)$ is calculated as 115 and 83 $\Omega \cdot$cm for the HfO_2 and NON TFTs, respectively. The difference in $R_{\rm SD}$ should be attributed to the different surfaces and/or interfaces of the channel/electrodes, since the materials and growth process of the channel and electrodes are identical for TFTs. The AFM measurement revealed that the rms roughness values are 3.08 and 3.60 nm for the α-IGZO on HfO_2 and the α-IGZO on NON, respectively. Thus, the reduced S/D contact resistivity resulting from the improved channel/source (drain) interface can be confirmed.

The TFT with the NON tristack dielectrics shows superior electrical characteristics compared to the HfO_2 TFTs, such as saturation mobility, ON/OFF-current ratio, and subthreshold swing, which can be seen in Table I. All these enhanced performances should be ascribed to the inserted HfO_xN_y interlayers between the Si gate and HfO_2 and between the HfO_2 and the α-IGZO channel, which improve the interface properties by suppressing the growth of the low-κ interface layer. Comparing with the α-IGZO TFT with the HfO_xN_y gate dielectric [7], the gate leakage and subthreshold properties have been improved with the NON gate dielectric.

IV. Conclusion

In conclusion, we have manufactured α-IGZO TFTs using $HfO_xN_y/HfO_2/HfO_xN_y$ as the tristack gate dielectric, and their electrical characteristics have been investigated by comparing them to the TFTs with the HfO_2 gate dielectric only. The experimental results have shown superior performance that has been achieved for α-IGZO TFTs with the NON dielectric, such as increased mobility, decreased gate leakage, improved subthreshold swing, and enhanced gate bias stressing reliability, which are all attributed to the improved properties of both the Si gate/dielectric and dielectric/active channel interfaces by inserting the HfO_xN_y interlayer. Furthermore, the S/D contact resistivity is reduced by improving the interfaces between the channel and metal S/D electrodes.

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