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Fabrication and electrical properties of metal-oxide semiconductor capacitors based on polycrystalline p-Cu_xO and HfO_2/SiO_2 high-κ stack gate dielectrics

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ABSTRACT

Polycrystalline p-type Cu_xO films were deposited after the growth of HfO_2 dielectric on Si substrate by pulsed laser deposition, and Cu_xO metal-oxide-semiconductor (MOS) capacitors with HfO_2/SiO_2 stack gate dielectric were primarily fabricated and investigated. X-ray diffraction and X-ray photoelectron spectroscopy were applied to analyze crystalline structure and Cu^+/Cu^{2+} ratios of Cu_xO films respectively. SiO_2 interlayer formed between the high-κ dielectric and substrate was estimated by the transmission electron microscope. Results of electrical characteristic measurement indicate that the permittivity of HfO_2 is about 22, and the gate leakage current density of MOS capacitor with 11.3 nm HfO_2/SiO_2 stack dielectrics is $\sim 10^{-4}$ A/cm^2. Results also show that the annealing in N_2 can improve the quality of Cu_xO/HfO_2 interface and thus reduce the gate leakage density.

1. Introduction

The copper oxide thin films are widely researched due to their potential applications in modern technology. Two crystalline forms of cuprous oxide (Cu_2O) and cupric oxide (CuO) exist together generally. Cu_2O is an oxide semiconductor with a direct band gap of 2.0–2.6 eV and a cubic crystal structure [1]. CuO have a low direct bandgap of 1.2–1.4 eV [2], and its crystal structure is monoclinic. Cu_2O and CuO can be controlled by the oxidation–reduction process during deposition or post deposition annealing [3]. Different techniques such as electrodeposition [4], thermal evaporation [5], thermal oxidation [6], radio frequency magnetron sputtering [7], pulsed laser deposition [8], and molecular beam epitaxy [9] have been used for the growth of copper oxide thin films.

Copper oxides attract much interest for the fabrication of optoelectronic devices, such as visible photodetector [10] and transistors [6,11–13], especially for transistors due to its unique p-type property. However, the gate dielectrics of obtained transistors are SiO_2 and Al_xO, and the thicknesses of dielectrics are all above 150 nm [11–13], in order to adapt the higher packing densities and less power consumption, device dimension should be scaled down, high-κ gate dielectrics have to be utilized to decrease gate leakage. Inspiring by the deposition of high-κ gate dielectrics, such as ZrO_2 [14] and HfO_2 [15] on Si or Ge substrate, $Cu_xO/HfO_2/SiO_2/\ p^+$ Si inverted MOS capacitors with p^+ Si as back gate were fabricated in this work. The experimental results exhibited good performances for MOS device, such as small physical thickness, high permittivity of gate dielectric, and low gate leakage current density.

2. Experimental details

Substrate used was p^+ silicon wafer (100) with 10 mm × 10 mm × 0.5 mm. The wafer was cleaned using the standard RCA technique. The oxide layer on silicon surface was removed by diluted HF solution. Pulsed laser deposition (PLD) was applied to prepare films, using a KrF excimer laser, wavelength was 248 nm, pulse duration was ~20 ns, pulse frequency was 7 Hz, and laser power density at the target surface was 2 mJ/cm^2. The laser beam was focused onto a rotating target at a 45° angle of incidence. The target was about 50 mm from the substrate which was put onto a rotating holder to improve the uniformity of the film. Prior to the deposition, the chamber was vacuumed to the based pressure of 1×10^{-4} Pa. The high-κ HfO_2 dielectric was first deposited on Si substrate in pure O_2 with a ceramics HfO_2 target having a purity of 99.99%, and substrate was kept at room temperature. Subsequently, Cu_xO film was *in situ* deposited on HfO_2/silicon at substrate temperature 700 °C, with a Cu metal target (4 N), and an oxygen partial pressure of 0.6 Pa [13]. The deposition rate as well as the nominal film thickness was monitored with a quartz crystal thickness monitor (TM-400, Maxtek, USA). The thicknesses of Cu_xO film and HfO_2 film are about 120 nm and 9 nm

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respectively, which have been checked by a VASE Series Ellipsometer and good agreements have been obtained. In order to study the effects of annealing on device performance, one sample was annealed at 750 °C for 300 s in N_2 ambient with a flow rate of 100 ml/min. Finally, Al was thermally evaporated and patterned as contact electrode with an area of 3.14×10^{-4} cm^2, and followed by forming-gas annealing at 300 °C for 20 min.

The X-ray diffraction (XRD) patterns were recorded with Bruker AXS X-ray diffractometer (D8 Advance) using Cu Kα radiation at 40 kV and 40 mA. Cu^+/Cu^{2+} ratios of copper oxide films were measured by X-ray photoelectron spectroscopy (XPS, VG Multilab2000). The XPS analysis was performed with all peaks referenced to C 1s at 284.6 eV. Film surface morphologies were observed by atomic force microscopy (AFM, SPM-9500 J3, Shimadzu, Japan) in the Tapping Mode in air. Transmission electron microscopy (TEM) was employed to evaluate the thickness of SiO_2 layer. The model of the TEM machine was Philips Tecnai G2 20 STWIN with a maximum resolution of ~0.2 nm and an operating voltage of 200 kV. Preparation of a TEM sample was as follows: 1) two small pieces (~2 mm×6 mm) of a wafer were face-to-face pasted together with glue, and then one of the cross sections was polished by a grinding machine; 2) with the polished cross section facing down, the sample was stuck at the center of a copper ring with a 0.6 mm-diameter hole; 3) after the sample was grinded down to several microns thick, ion beam milling was used to further reduce the sample thickness to ~10 nm, which was critical for obtaining clear image. Lastly, the sample was placed into a TEM machine to take photo on its cross section. High-frequency (HF, 1 MHz) capacitance–voltage (C–V) characteristics were measured at room temperature using HP4294A precision LCR meter. Gate leakage current was measured by a Keithley 4200 precision semiconductor parameter analyzer, gate voltage was applied on the p^+ Si back gate. All electrical measurements were carried out under a light-tight and electrically-shielded condition.

3. Results and discussion

The AFM images of the samples are shown in Fig. 1(a) and (b). The root main square roughness of the as-deposited copper oxide film is found to be 6.87 nm, and that of annealed sample is slightly smaller (4.51 nm), which probably suggests that the grains are distributed more uniformly by annealing due to increasing surface energy. Typical XRD patterns of copper oxide films are shown in Fig. 1(c). The diffraction peaks located at $2\theta=36.3°$ and 42.3° correspond to (111) and (200) planes of cubic Cu_2O phase (ICCD File: 05-0667; space group #224), the other diffraction peaks located at $2\theta=32.2°$ and 35.3° belong to (110) and ($\bar{1}$11) planes of CuO with monoclinic phase (ICCD File: 45-0937; space group #15), and no obvious peak of Cu can be found, which denotes that the films are polycrystalline including compound of Cu^{2+} and Cu^+. The Cu $2P_{3/2}$ core level was employed to investigate the presence of different oxidation states of copper. The Cu $2P_{3/2}$ peak can be deconvoluted into two peaks [5], the XPS binding energy related to Cu_2O is 933.4 eV, and the position of the peak that corresponded to CuO is 935.1 eV. The Cu^+/Cu^{2+} ratios obtained from the deconvolution of Cu $2P_{3/2}$ peaks are roughly calculated as 52% and 63% for as-deposited and annealed samples respectively, which indicates that annealing in N_2 can partly reduce Cu^{2+} to Cu^+. Maybe pure Cu_2O can be obtained by further improving annealing conditions.

Fig. 2 shows the TEM images of the Cu_xO MOS capacitors with HfO_2/SiO_2 stack gate dielectrics. Because the oxidization of silicon is inevitable, not only during deposition of HfO_2 or Cu_xO, but also during annealing, what is more, residual O_2 in N_2 and/or in furnace chamber is sufficient to oxidization of silicon. Therefore, the dielectric layers for MOS capacitors are not lone HfO_2, it included SiO_2 practically, as being described in the inset of Fig. 3. SiO_2 interlayer between the high-κ dielectric and silicon substrate is estimated from the TEM photographs as 2.3 nm and 3.4 nm for as-deposited and annealed samples respectively.

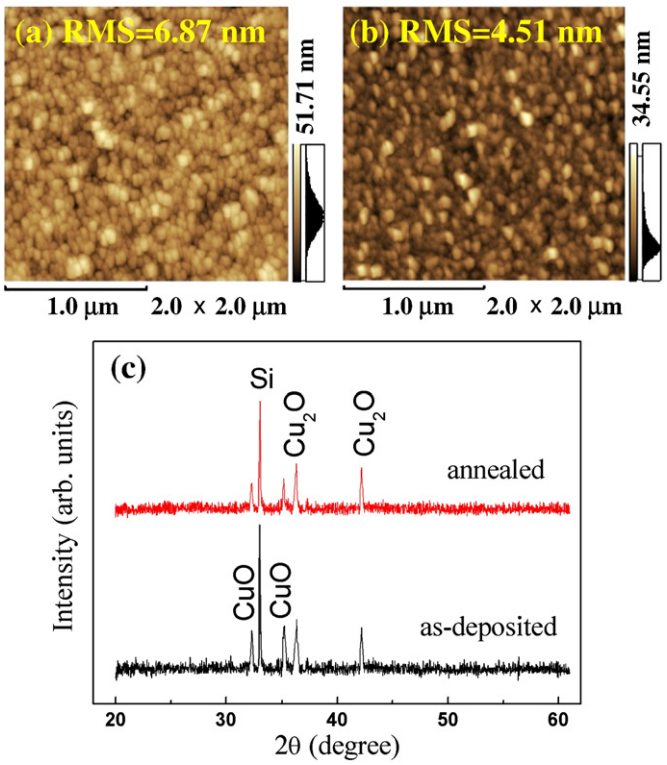

Fig. 1. AFM images of (a) as-deposited and (b) annealed copper oxide films prepared at 700 °C and 0.6 Pa O_2, and (c) XRD pattern of the films.

Fig. 3 depicts the typical high-frequency (1 M Hz) C–V curves under dark condition for samples. The C–V curves indicate the p-type semiconductor behavior of Cu_xO films, when a negative gate voltage is applied to capacitor, an accumulation layer of positive carriers (holes) was formed at the Cu_xO semiconductor surface. Bulk and/or thin films Cu_xO show an intrinsic p-type character due to the presence of copper vacancies introducing an acceptor level at about 0.3 eV above the valence band [16]. Cu_xO is a compensated material with a compensation ratio N_A/N_D (N_A and N_D are the acceptor and donor densities respectively) between 1 and 10, the acceptor density estimated from the hole concentration $p(T)$ curves (data not shown) is in the range of 10^{14}–10^{15} cm^{-3}. The calculation equation is as Eq. (1), Where N_A and N_D^+ are the concentrations of acceptors and ionized donors, E_A is the acceptor energy level, calculation details are according to Mattiga et al. [17]).

$$p(T)=-\frac{1}{2}\left(N_D^+ + \frac{N}{e^{E_A/kT}}\right)+\frac{1}{2}\sqrt{\left(N_D^+ + \frac{N_v}{e^{E_A/kT}}\right)^2+4\frac{N_v}{e^{E_A/kT}}(N_A-N_D^+)}. \quad (1)$$

As can be seen from Fig. 3, sweeping in both directions, small hysteresis is observed due to interface and near-interface trap densities and the mobile ions in dielectric. The trap states should be attributed to intrinsic defect of Cu_xO and/or reaction between Hf and Cu during the deposition of Cu_xO film. For annealed sample, the accumulation capacitance (gate dielectric capacitance, C_{ox}) decreased slightly related to the increment of the thickness of SiO_2 during the annealing. It was also noticed that the V_{fb} is positive, which suggested that there is a significant negative oxide charge in the gate dielectric. And the V_{fb} shifts to the negative direction after anneal, indicating that annealing could suppress the negative oxide charge during the

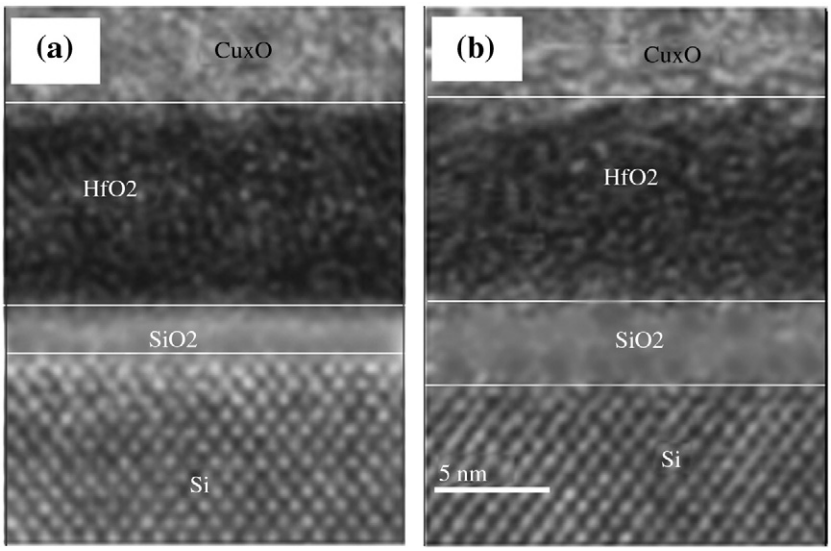

Fig. 2. TEM images of (a) as-deposited and (b) annealed HfO_2/SiO_2 stack gate dielectric on Si substrate.

thermal process by introducing positive oxide charges associated with N incorporation [18]. Negative oxide charges enhanced the accumulation of holes at the interface due to induce positive charges on the surface of the semiconductor channel. As reflected from the shift of the *C–V* curve, to realize the inversion of holes on the interface, a high positive voltage bias needs to be applied. The induction of positive charges on the surface also leads to the carrier scattering in the channel and thus degrade mobility. The oxide charge density Q_{ox} can be estimated as [19], where the φ_{ms} is the work–function difference between Al and p^+ silicon, C_{ox} is the accumulation capacitance, and V_{fb} is the flatband voltage. Therefore, the oxide charge density is estimated to be $1.2–1.5\times10^{13}$ cm^{-2}.

The physical thickness (t_{ox}) of gate dielectrics, capacitance equivalent thickness (CET), flatband voltage (V_{fb}), and the interface-state density (D_{it}) extracted from the 1 M Hz *C–V* curves are listed in Table 1. Total physical thicknesses of stack dielectrics t_{ox} are 11.3 nm and 12.5 nm, respectively, measured by multiwavelength ellipsometer, in which the Cauchy model and light wavelengths ranging from 400 to 1000 nm were used to obtain the film thickness. $CET = A\times\kappa_{SiO_2}\kappa_0/C_{ox}$, where κ_{SiO_2} and κ_0 is the permittivity of SiO_2 and vacuum respectively. V_{fb} is determined from the flatband capacitance (C_{fb}). Approximate D_{it} at midgap is extracted by the Terman method for comparison purpose only [20]. Obviously, the annealed sample has the smaller C_{ox}, and thus the larger CET, mainly

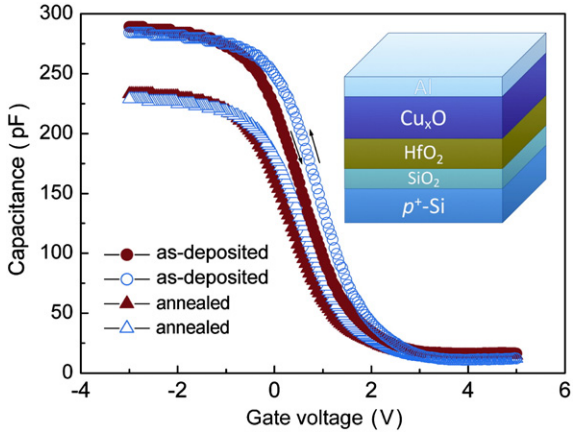

Fig. 3. High-frequency (1 MHz) *C–V* curves of as-deposited and annealed samples. The MOS structure is shown in the inset.

due to the increment of thickness of SiO_2 during annealing in N_2. Higher D_{it}'s ($\sim10^{12}$ eV^{-1} cm^{-2}) are found for all samples, indicating a large amount of defects of Cu_xO film and HfO_2/Cu_xO interface, because the D_{it} is the combined effect of oxide charge, mobile ions, border trap charge, and/or near-interface defect charge near the Fermi level. This D_{it} is of the same order of magnitude as the value of the MOS device with HfO_2 on GaAs [21]. The annealed sample has a relatively low D_{it} than that of as-deposited sample, possibly results from the nitrogen incorporation into the films during annealing in N_2, by reason of nitrogen incorporation in HfO_2 can suppress impurity penetration and improve interface quality [22]. The relative permittivity κ_{ox}'s of the gate stack dielectrics, as calculated by $\kappa_{SiO_2}\times(t_{ox}/CET)$, are listed in Table 1 too, the κ value of the annealed sample is lower than that of the as-deposited sample due to increased thickness of SiO_2 during annealing process. It should be noted that the permittivity κ_{ox} is the equivalent κ value of dielectric and interlayer. Based on the formula of $\kappa_{ox}=\kappa_{SiO_2}\times t_{ox}/CET = t_{ox}/(t_{SiO_2}/\kappa_{SiO_2}+t_{HfO_2}/\kappa_{HfO_2})$, where κ_{HfO_2} is the permittivity of HfO_2 layer, t_{SiO_2} and t_{HfO_2} are physical thicknesses of SiO_2 and HfO_2 layers respectively, κ_{HfO_2} can be calculated as ~22, which is slightly smaller than the κ value of HfO_2 on Ge (~25) reported by Dimoulas et al. [15], but higher than the result of HfO_2 on IGZO (~18) reported by Nomaru et al [23], and far above that of HfO_2 on GaAs (~8.8) [21].

The gate leakage properties of samples have been shown in Fig. 4. The samples have gate leakage current of $\sim10^{-4}$ A/cm^2 at $V_g=-1$ V (accumulation), which is of the same order of magnitude as that of MOS device with HfO_2 on ZnO ($t_{ox}=25$ nm, nearly double the thickness of our samples) [24], indicating super insulator properties of HfO_2/SiO_2 stack gate dielectric. The leakage current of annealed sample is smaller than that of the as-deposited sample, obviously, which is ascribed to larger thickness of stack dielectric and better dielectric properties annealing in N_2 [25].

Table 1
Physical oxide thickness, gate-oxide capacitance, capacitance equivalent thickness, flatband voltage, interface-state density and equivalent permittivity of the samples.

Samples	t_{ox} (nm)	C_{ox} (pF)	CET (nm)	V_{fb} (V)	D_{it} (cm^{-2} eV^{-1})	κ_{ox}
As-deposited	11.3	289	3.74	2.63	3.4×10^{12}	11.8
Annealed	12.5	226	4.78	2.21	1.6×10^{12}	10.2

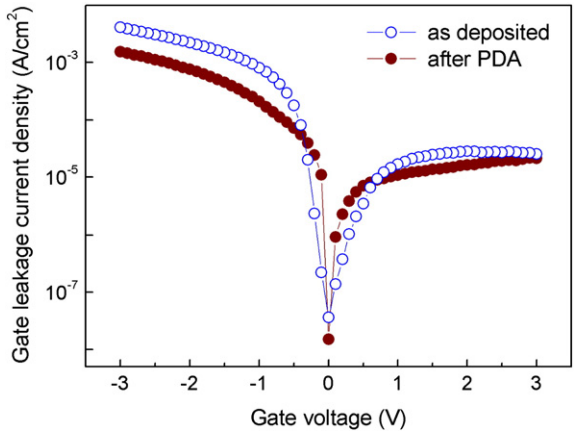

Fig. 4. Gate leakage current density as a function of gate voltage for as-deposited and annealed samples.

4. Conclusions

In summary, polycrystalline p-Cu_xO film and high-κ HfO_2 gate dielectric have been deposited on p^+ Si substrate by PLD method. Results indicate that polycrystalline Cu_xO is a p-type semiconductor. And superior electrical properties of MOS capacitors have been achieved, such as physical thickness of stack dielectrics is about 12 nm, gate leakage current density is of $\sim 10^{-4}$ A/cm^2 at $V_g = -1$ V, equivalent κ value of dielectric is above 10. Experimental results also show that 750 °C annealing in N_2 can decrease the interface state density, and reduce gate leakage. However, higher D_{it}'s of as-deposited and annealed sample reveal that further study is needed to improve the interface quality.

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